



Applicant:

Hunt Hang Jiang, et al.

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For:

Structure and Method for Depositing

Solder Bumps on a Wafer

Art Group Unit:

2812

Examiner:

Unknown

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**CERTIFICATE OF** MAILING/TRANSMISSION (37 C.F.R. § 1.8A)

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## INFORMATION DISCLOSURE STATEMENT PURSUANT TO 37 C.F.R. §1.56 AND §§1.97-1.98

Commissioner for Patents Washington, D.C. 20231

Sir:

The citations listed on the enclosed PTO-1449 Form are submitted under 37 C.F.R. §§1.97 and 1.98, and in compliance with the duty of disclosure as defined in 37 C.F.R. §1.56. The Examiner is requested to make these citations officially of record in the application. The items of information contained in the Information Disclosure Statement are being submitted before receipt of the first Office Action on the merits for the above-identified application. Accordingly, pursuant to 37 C.F.R. §1.97, no fee or certification is required.

INFORMATION DISCLOSURE STATEMENT Page 2

This Information Disclosure Statement Under 37 C.F.R. §1.56 is not to be construed as a representation that any of the listed citations establishes, by itself or in combination with other information, a prima facie case of unpatentability of any claim in the above-identified application. Additionally, this Information Disclosure Statement is not to be construed as a representation that a further search of the art has been made by Applicants, or that additional information relevant to the examination of this application does not exist unbeknownst to Applicants.

Respectfully submitted,

John W/Carpenter Registration No.: 26,447

August 14, 2001 **COUDERT BROTHERS** 600 Beach Street, 3<sup>rd</sup> Floor San Francisco, CA 94109 (415) 409-2900 (tel.) (415) 409-7400 (fax)